

YC1292VP LDMOS TRANSISTOR

Document Number: YC1292VP
Preliminary Datasheet V1.0

1000W, 50V High Power RF LDMOS FETs

Description

The YC1292VP is a 1000-watt, high performance, internally matched LDMOS FET, designed for multiple applications with frequencies 0.9 to 1.3GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as Avionics applications.

It is recommended to use this device under pulse condition. Please ensure adequate cooling if running at CW.

- Typical Narrow Band Performance (on Yingtron test fixture with device soldered):

$V_{DD} = 50\text{ V}$, $I_{DQ} = 100\text{ mA}$, Pulse width:20uS, duty cycle: 50%,

Freq(MHz)	P3dB(W)	EFF(%)@P3dB	Gp@ P3dB (dB)
1030	1200	50	13

- Typical Performance (on Yingtron test fixture with device soldered):

$V_{DD} = 50\text{ V}$, $I_{DQ} = 100\text{ mA}$, Pulse width:20uS, duty cycle: 10%,

Freq(MHz)	P1dB(dBm)	P3dB(dBm)	EFF(%)@P3dB	Gp@ P1dB (dB)
960	59.1	59.9	54.2	14.6
1000	59.2	60.0	54.5	14.5
1050	59.3	60.0	54.1	13.5
1080	59.4	59.9	52.8	12.8
1150	59.2	59.8	48.9	13.1
1215	59.1	59.8	48.7	15.3



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 1000W Pout, Pulse width: 20us, duty cycle: 2%,	$R_{\theta JC}$	0.02	°C/W

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$V_{DD}=50\text{ V}$, $I_{DQ} = 100\text{ mA}$		
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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Breakdown Voltage ($V_{GS}=0\text{V}$; $I_D=100\mu\text{A}$)	V_{DSS}		115		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$)	I_{DSS}			10	μA
Gate--Source Leakage Current ($V_{GS} = 6\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}			1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage ($V_{DD} = 50\text{ V}$, $I_{DQ} = 100\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$		3.05		V

Functional Tests (In Yingtron test fixture, 50 ohm system) : $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 1030\text{ MHz}$, Pulse CW Signal Measurements. (Pulse Width=20 μs , Duty cycle=50%)

Power Gain @ P3dB	G_p		13		dB
3dB Compression Point	P3dB		1200		W
Drain Efficiency@P3dB	η_D		50		%
Input Return Loss	IRL		-7		dB

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Reference Circuit of Test Fixture Assembly Diagram

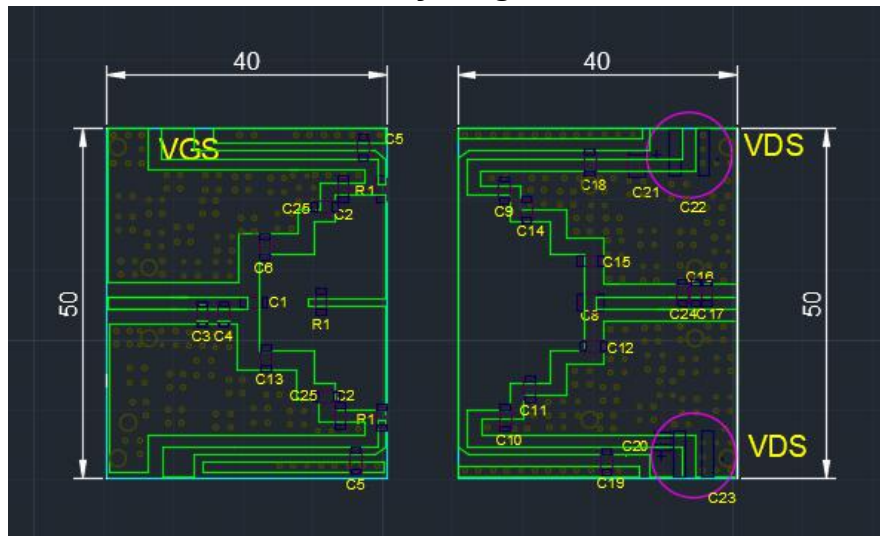


Figure 1. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

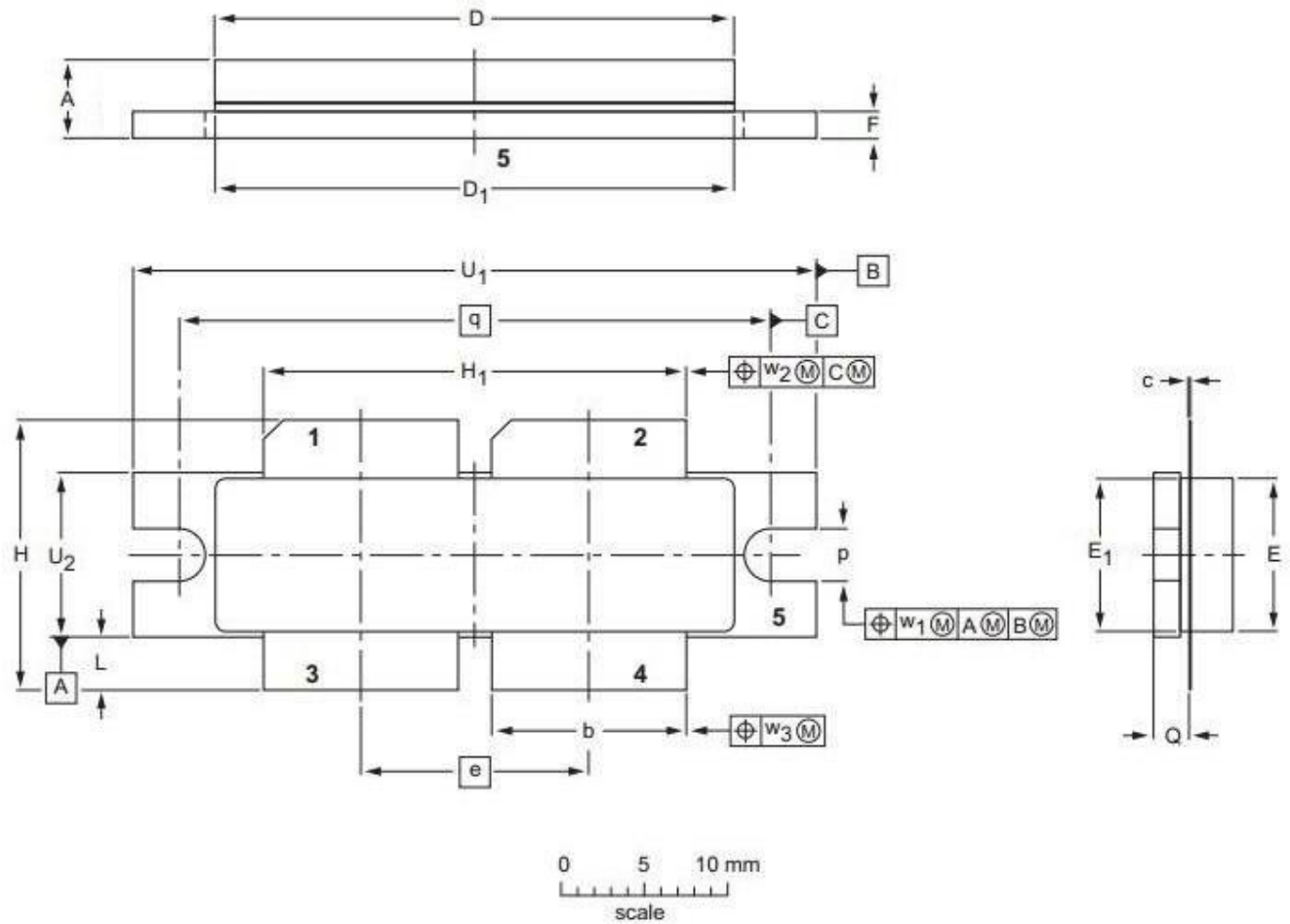
Component	Description	Suggested Manufacturer
C2	Ceramic Capacitor, 8.2pF	ATC800B
C6	Ceramic Capacitor, 3.3pF	ATC800B
C9 C10	Ceramic Capacitor, 4.7pF	ATC800B
C3 C4 C11 C14 C17	Ceramic Capacitor, 2.4pF	ATC800B
C13	Ceramic Capacitor, 6.2pF	ATC800B
C12 C15	Ceramic Capacitor, 3.9pF	ATC800B
C25	Ceramic Capacitor, 1.2pF	ATC600F
C24	Ceramic Capacitor, 0.8pF	ATC600F
C1 C5 C8 C18 C19	Ceramic Capacitor, 68pF	ATC800B
C16	Ceramic Capacitor, 0.3pF	ATC800B
C20 C21	Ceramic Capacitor, 10uF	1210, X7R
C22 C23	Electrolytic Capacitor, 220uF, 63V	
R1	Chip Resistor, 10 Ω	
PCB	0.762mm [0.030"] thick, $\epsilon_r=3.48$, Rogers RO4350B, 1 oz. copper	

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1, 2—DRAIN, 3, 4—GATE, 5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₂
Mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
Inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2019/01/03	Rev 1.0	Preliminary Datasheet Creation

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