YC1040VP LDMOS TRANSISTOR

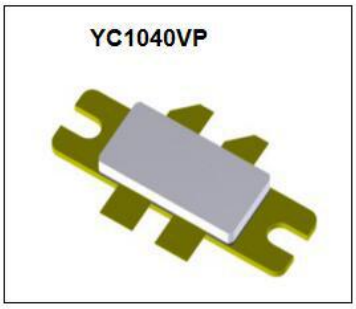
Document Number: YC1040VP
Preliminary Datasheet V1.1

400W, 50V High Power RF LDMOS FETs

Description

The YC1040VP is a 400-watt, high performance, internally matched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies 0.5 to 1GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as UHF TV and Aerospace applications.



- Typical performance(on 0.5-1GHz wideband test board with device soldered)

Signal：pulse CW, pulse width:100us，duty cycle:10%, V_{GS} =2.99V, V_{DD} =50V, I_{DQ} =120mA

Freq (MHz)	P_{SAT} (dBm)	G_P (dB)	η (%)
500	57.4	14.2	47
600	57.8	16.6	64
700	56.5	14.8	57
800	56.1	15.4	43
900	56.7	15.9	45
1000	56.0	15.5	56

- Typical performance (on 915MHz narrow band test board with device soldered)

V_{GS}=2.97V, V_{DD} =50V, I_{DQ} =100mA Frequency 915MHz

Signal	P_{SAT} (dBm)	G_P (dB)	η (%)
10% 100us	57.3	17.8	60.0
20% 100us	57.4	17.3	58.5
20% 1ms	57.0	16.9	56.5

- Typical performance (on 860MHz narrow band test board with device soldered)

Freq (MHz)	V_{DD}=50V, I_{DQ}=200mA, Pulse Signal			Vds=50V, I_{DQ} =500mA, W-CDMA Signal PAR=7.6dB			
	P_{SAT} (dBm)	G_P (dB)	η (%)	P_{AVG} (dBm)	G_P (dB)	η (%)	$ACPR_{\_5M}$ (dBc)
860	56.8	17.7	62.7	50	20	35.7	-32

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600μA)	$V_{GS(th)}$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V

Load Mismatch (In Yingtron Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 915MHz, pulse width:100us, duty cycle:20%

VSWR 10:1, at 500W Pulsed CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

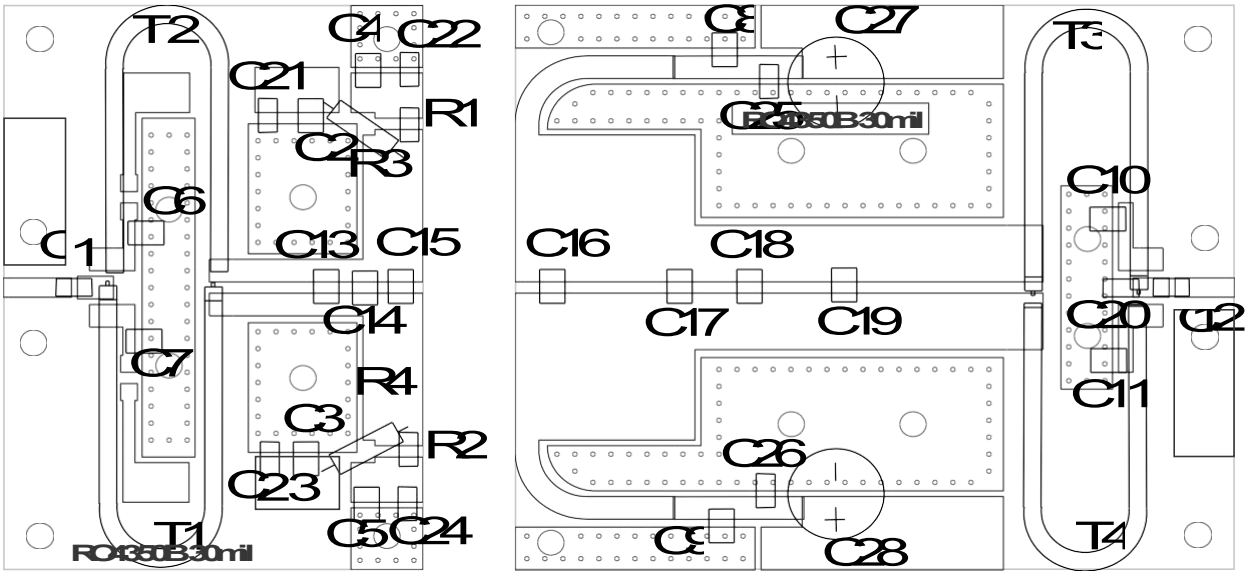


Figure 1. Test Circuit Component Layout (860M Narrow Band)

Table 5. Test Circuit Component Designations and Values

Part	description	Model
C1~C12	47PF	ATC800B
C13	1.5PF	DLC70B
C14,C19	6.8PF	ATC800B
C15	10PF	ATC800B
C16,C17,C20	2.2PF	DLC70B
C18	4.7PF	ATC800B
C21~C26	10UF	100V/10UF
C27,C28	470UF	63V/470UF
R1,R2	9.1Ω	1206
R3,R4	100Ω	1W/100Ω
T1,T2,T3,T4	25Ω,50mm	SF-086-25
PCB	0.762mm [0.030"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper	

TYPICAL CHARACTERISTICS

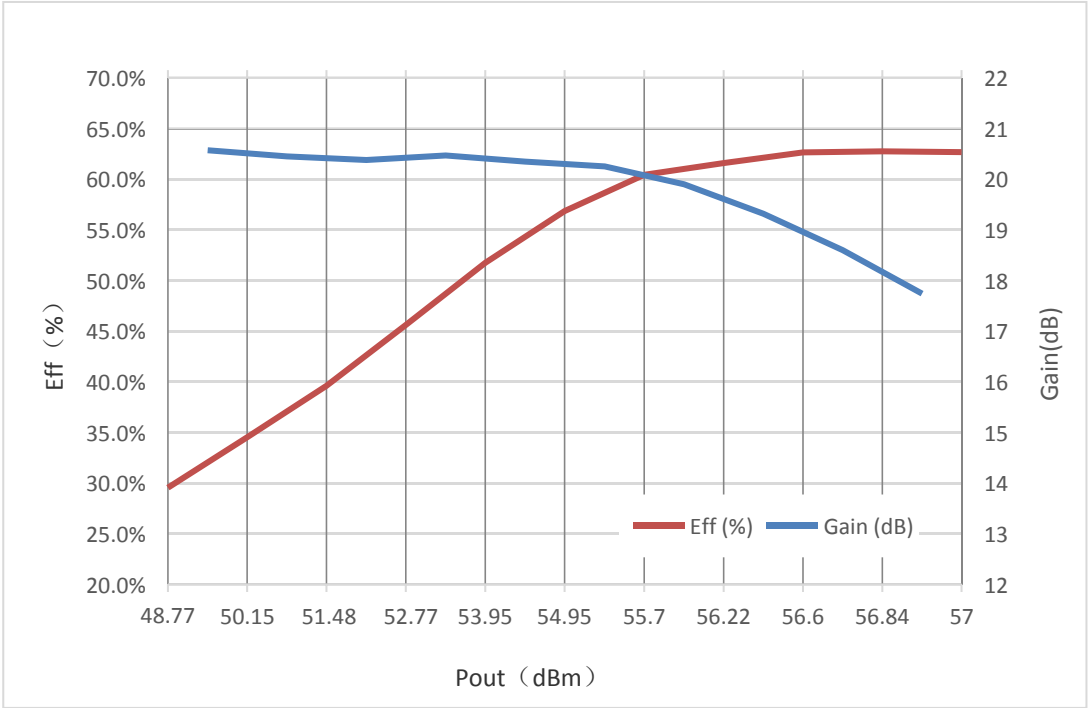
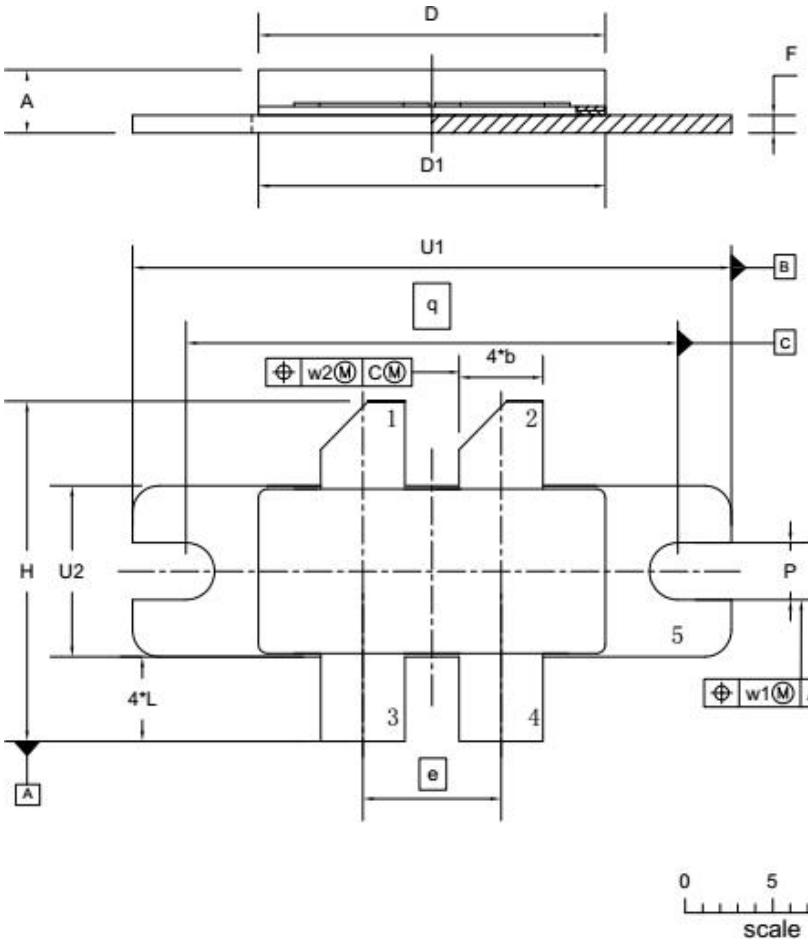


Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power（860MHz Narrow Band）

Package Outline

Eared Flanged Ceramic Package; 2 mounting holes; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.93 4.67	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/6/27	Rev 1.0	Preliminary Datasheet Creation
2019/12/09	Rev 1.1	Preliminary Datasheet