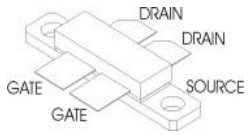
YC0560VPX LDMOS TRANSISTOR

Document Number: YC0560VPX
Preliminary Datasheet V1.0

550W, 50V High Power RF LDMOS FETs

YC0560VPX



Description

The YC0560VPX is a 550-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.6 GHz.

It is the thermally enhancement of its peer YC0560VPX.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical performance(on 325MHz test board with device soldered):
  V_{DD} = 50 Volts, I_{DQ} = 95 mA, CW.

Freq (MHz)	Pout (dBm)	Pout (W)	Gain (dB)	Eff (%)
325	55.7	368	22.3	65.7
325	56.0	417	21.8	68.5
325	56.6	459	21.2	72.8
325	57.0	495	20.5	72.6
325	57.2	525	19.7	73.4
325	57.4	550	18.9	74.4

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit

Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.30	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0Ma	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	— —	— —	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	— —	— —	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	— —	— —	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600μA)	$V_{GS(th)}$	— —	2.65	— —	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	— —	3.25	— —	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)		189		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		158		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		46.8		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		1.24		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 325MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 500W Pulsed CW Output Power	No Device Degradation

Figure 1: CW gain and Efficiency as function of output power at 325MHz (Vds=50V, Idq=95mA)

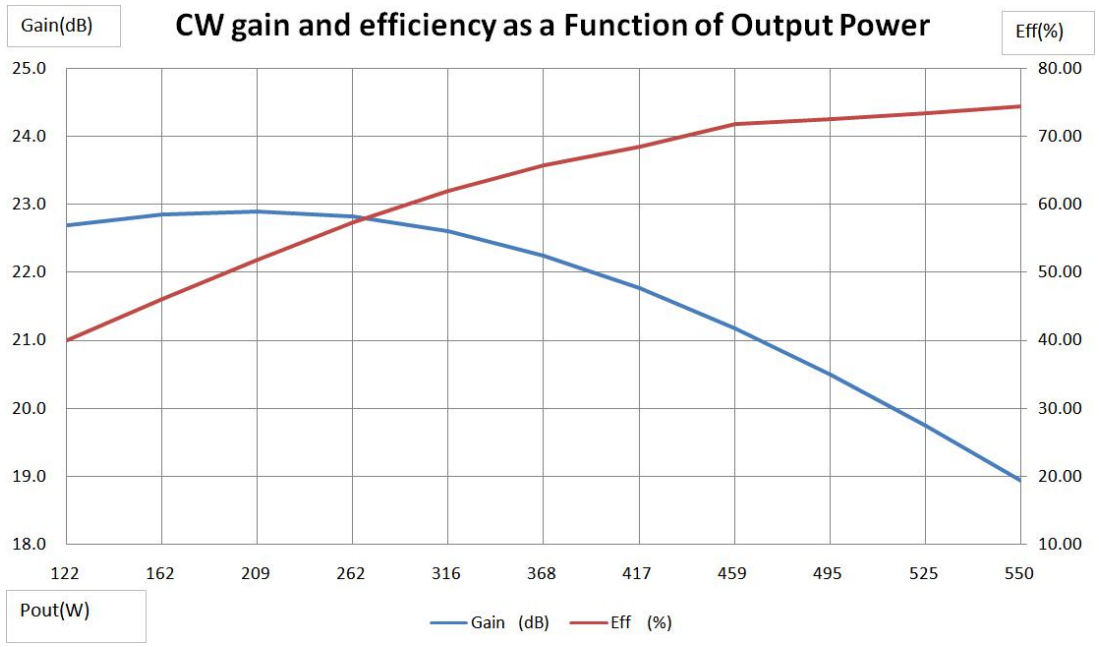
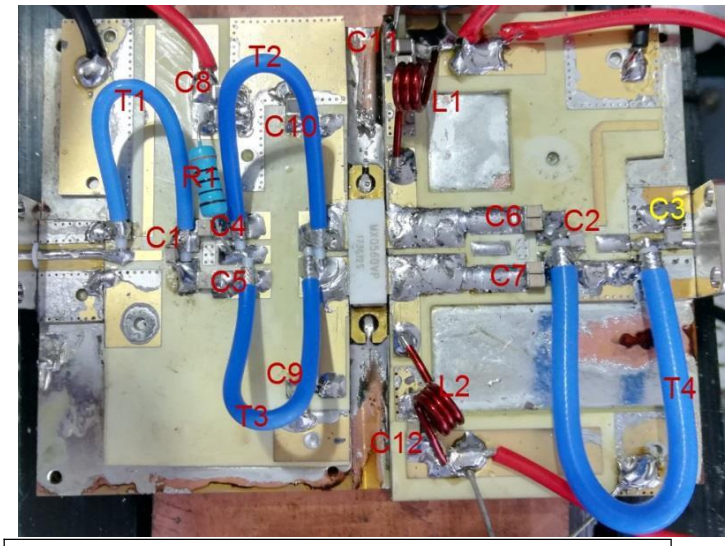


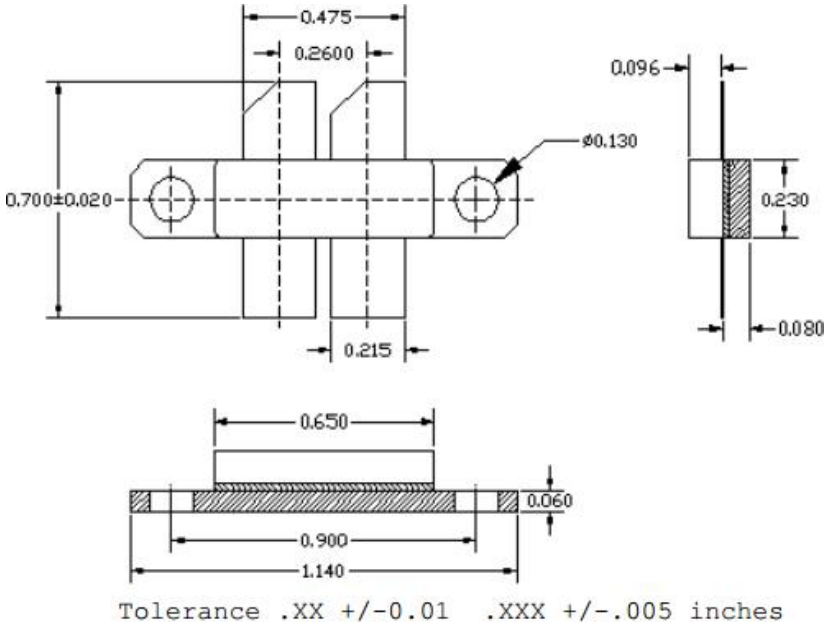
Figure 2: Photo of test fixture and bill of materials

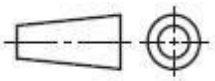


BOM		
T1	50Ω 60mm	
T2,T3	25Ω 70mm	
T4	25Ω 93mm	
C1,C2	18PF	ATC800B
C3	3.9PF	ATC800B
C4,C5	270PF	ATC800B
C6,C7	270PF x2	ATC800B
C8,C9,10,C11,C12	10UF	
L1,L2	4turns	Diameter=5mm
R1	300Ω	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					**03/12/2013**

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/3/28	Rev 1.0	Preliminary Datasheet Creation

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