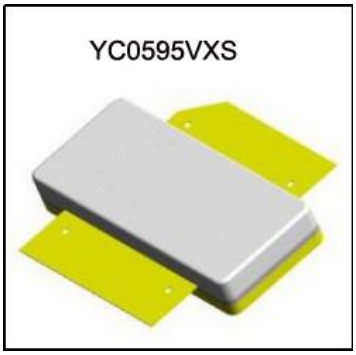
YC0595VXS*2 LDMOS TRANSISTORs

Document Number: MX0595VXS
Preliminary Datasheet V1.0

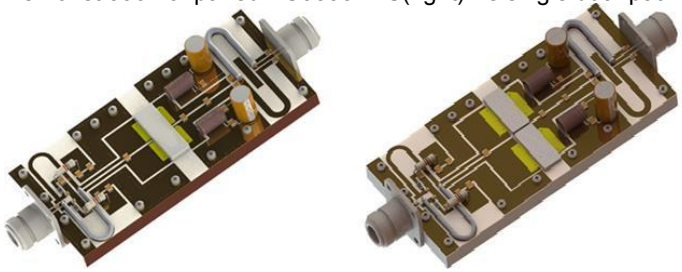
1600-1700W, 50V High Power RF LDMOS FETs

Description

The YC0595VXS itself is a 850-watt capable, high performance, unmatched single ended LDMOS FET, It is recommended to use paired YC0595VXS to enable 1600-1700W designed for commercial and industrial applications with frequencies HF to 250MHz. Compared to similar power level but in single dual-path packaged device, it offers better thermal management and easier maintenance.



Demonstration of paired YC0595VXS(right) Vs single dual-path device(left) at 250MHz.



- Typical performance(on 88-108MHz wideband test board with **YC0595VXS*2** devices soldered)

V_{DS}=50V,I_{DQ}=200mA, Pulsed CW, 10% duty cycle, 100us pulse width, tuned for efficiency

Freq(MHz)	P_{out}(W)	Pin(dBm)	Gain(dB)	η(%)
108	1600	43.8	18	79

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, 1600W Pulsed CW output,108MHz, 2 pcs of YC0595VXS combined, 10% duty cycle, 100us pulse width	RθJC	0.02	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

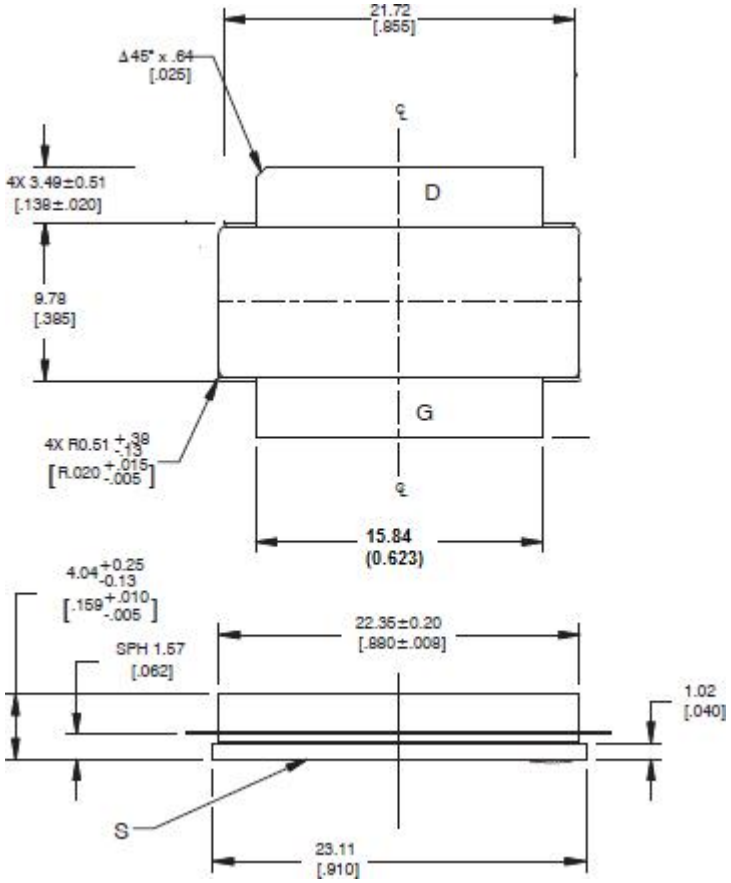
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600μA)	V_{GS}(th)	——	2.0	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 230 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.62	——	V

Load Mismatch (In Yingtron Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f = 108MHz, pulse width:100us, duty cycle:10%, 2 piece of YC0595VXS combined

Open and short, at 1600W Pulsed CW Output Power	No Device Degradation

Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2019/12/27	Rev 1.0	Preliminary datasheet

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