

YC188XR LDMOS TRANSISTOR

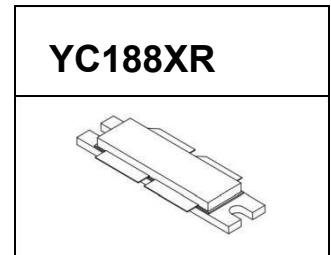
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Preliminary Datasheet

1300W, 50V High Power RF LDMOS FETs

Description

The YC188XR is a 1300-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 500MHz. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.



- Typical Performance (On Yingtron FM band fixture with device soldered, Power tuned):

$V_{DD} = 50$ Volts, $I_{DQ} = 200$ mA, CW, $P_{in} = 25$ W

Freq(MHz)	Pout(W)	Gain(dB)	Eff(%)
88	1320	18	78
98	1350	18	79
108	1330	17.5	77

- Recommended driver: YC1503V or YC1506VP
- Application board for 2-30/27/40/225/325MHz upon request

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 1300W CW, 50 Vdc, $I_{DQ} = 100$ mA	$R_{\theta JC}$	0.11	°C/W
Transient thermal impedance from junction to case $T_j = 150^\circ$ C; $t_p = 100$ us; Duty cycle = 20 %	Z_{th}	0.03	°C/W

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0mA$	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50V, V_{GS} = 0 V$)	I_{DSS}	---	---	1	μA
Gate—Source Leakage Current ($V_{GS} = 10 V, V_{DS} = 0 V$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 50V, I_D = 600\mu A$)	$V_{GS(th)}$	---	2.54	---	V
Gate Quiescent Voltage ($V_{DD} = 50 V, I_D = 200 mA$, Measured in Functional Test)	$V_{GS(Q)}$	---	3.17	---	V
Drain source on state resistance ($V_{DS} = 0.1V, V_{GS} = 10 V$) Each section side of device measured	$R_{ds(on)}$		80		m Ω
Common Source Input Capacitance ($V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz$) Each section side of device measured	C_{ISS}		600		pF
Common Source Output Capacitance ($V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz$) Each section side of device measured	C_{OSS}		140		pF
Common Source Feedback Capacitance ($V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz$) Each section side of device measured	C_{RSS}		2.2		pF

Reference Circuit of Test Fixture (88-108MHz)

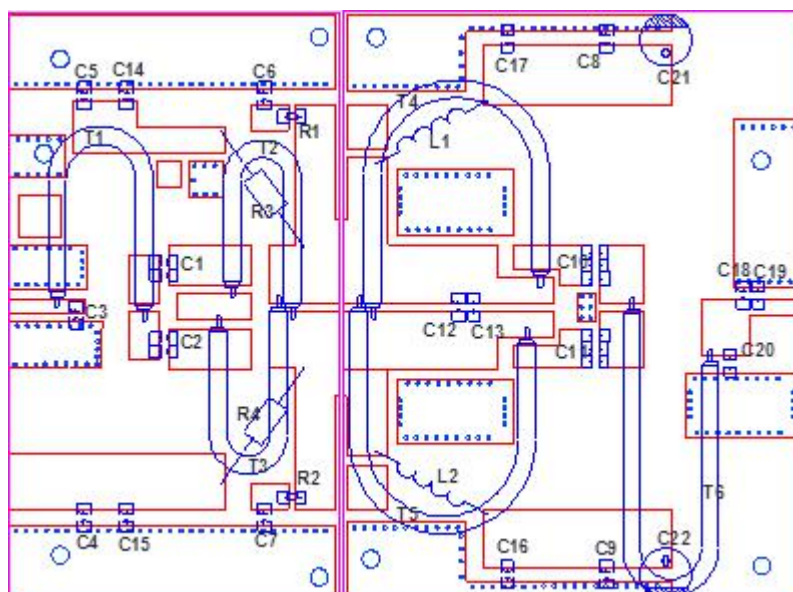


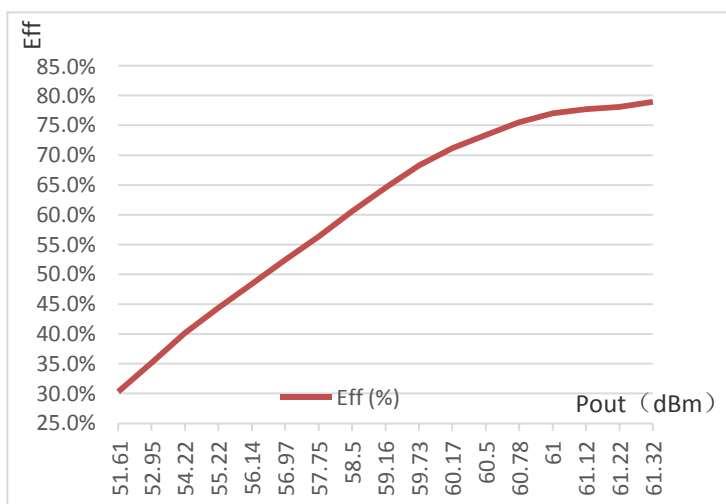
Figure 1. Test Circuit Component Layout

Part	description	Model
C1, C2, C6, C7, C10, C11, C16, C17	470PF	DLC70B
C3	1.5PF	DLC75D
C4, C5, C6, C7, C8, C9	10UF	100V/10UF
C10,C11	470PF*3	DLC70B
C12	4.7PF	DLC70B
C13	10PF	MIN02-002CC100J-F
C14~C17	1000PF	DLC70B
C18	2.2PF	DLC70B
C19,C20	3.3PF	DLC70B
R1,R2	39Ω*2	0805
R3,R4	470Ω	1W/470Ω
L1, L2	50nH	DIY
T1	50Ω,150mm	SF-086-50
T2,T3	25Ω,150mm	SFF-25-1.5
T4,T5	12.5Ω,170mm	SFF-12.5-1.5
T6	50Ω,200mm	RG402-3

TYPICAL CHARACTERISTICS

Figure 2: Power Efficiency as a Function of Pout

Vds = 50 V, Idq = 400 mA, TA = 25 °C, CW Frequency=100MHz

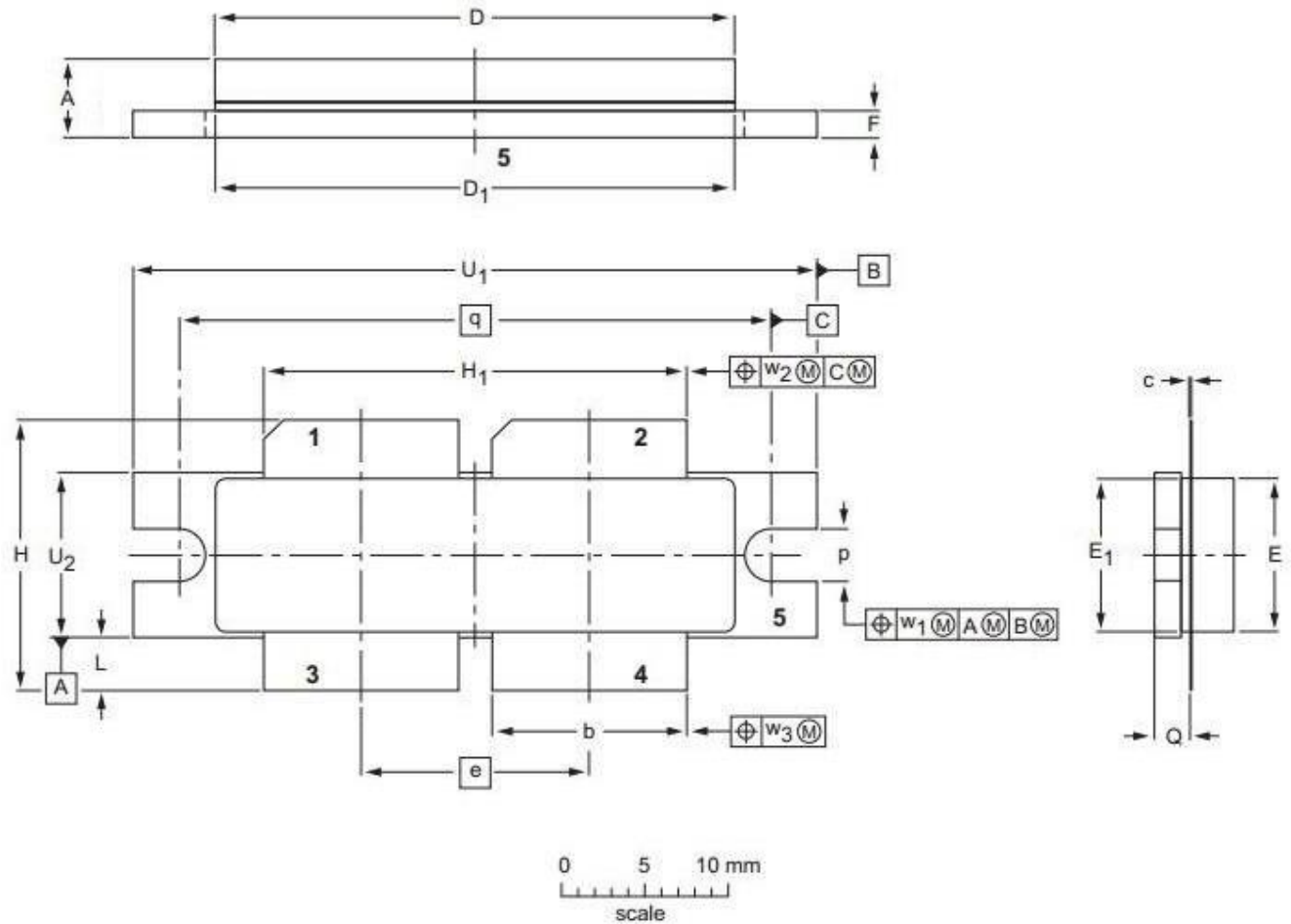


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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2019/12/17	Rev 1.0	Preliminary Datasheet

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