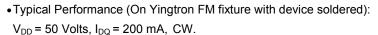
1000W, 50V High Power RF LDMOS FETs

Description

The YC051K1VPX is a 1000-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 500MHz. It is also featured with high ruggedness as well.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.



Freq (MHz)	Trade off	Pout(W)	Gain (dB)	Eff (%)
88-108	Power tuned	1120	18	75
88-108	Efficiency tuned	1020	20	79

• Typical Performance (On Yingtron narrow band fixture with device soldered): V_{DD} = 50 Volts, I_{DQ} = 1300 mA, CW.

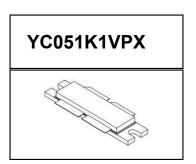
Freq(MHz)	eq(MHz) Pout(dBm) Gain(dB)		
1.6	56	23.3	52
5	56	22.8	58
10	56	21.5	59
15	56	21.3	59
20	56	22.2	56
25	56	23.4	53
30	56	23	51

• Typical Performance (On Yingtron narrow band fixture with device soldered): $V_{DD} = 50 \text{ Volts}$, $I_{DQ} = 1300 \text{ mA}$, 2-Tone CW Signal with Spacing 650Hz

Freq(MHz)	Pavg(dBm)	Gain(dB)	Eff(%)	IMD3(dBc)
1.6	53	23.6	40	-34
5	53	22.7	44	-33
10	53	21.6	45	-35
15	53	21.3	45	-36
20	53	22.2	43	-35
25	53	23.4	41	-33
30	53	22.9	39	-32.5

• Typical Performance (On Yingtron narrow band fixture with device soldered): V_{DD} = 50 Volts, I_{DQ} = 100 mA, Pulse CW: Pulse width=200uS, Duty Cycle=20%.

Freq(MHz)	P _{SAT} (W)	G _P (dB)	Eff(%)		
27	1072	24.5	70		



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Features

- · High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- · Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	125	Vdc
GateSource Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T,	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature	Dolo	0.15	°C/W
80°C, 1000W CW, 50 Vdc, IDQ = 100 mA	RθJC	0.15	- 5,744

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 $^{\circ}$ C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit	
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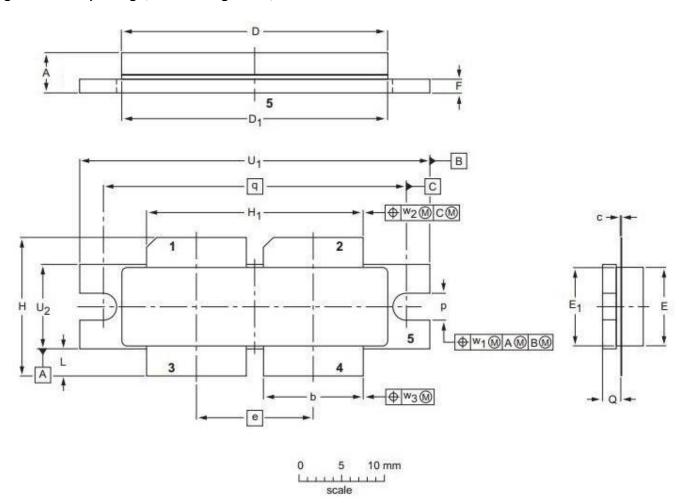
DC Characteristics

Drain-Source Voltage				
V _{GS} =0, I _{DS} =1.0mA	$V_{\text{(BR)DSS}}$	125		V
Zero Gate Voltage Drain Leakage Current				
$(V_{DS} = 50V, V_{GS} = 0 V)$	I _{DSS}	 	1	μΑ
Gate—Source Leakage Current				
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	I _{GSS}	 	1	μΑ
Gate Threshold Voltage				
$(V_{DS} = 50V, I_D = 600 \mu A)$	$V_{\text{GS}}(\text{th})$	 2.54		V
Gate Quiescent Voltage				
$(V_{DD} = 50 \text{ V}, I_D = 400 \text{ mA}, \text{Measured in Functional Test})$	$V_{GS(Q)}$	 3.1		V
Drain source on state resistance				
$(V_{DS} = 0.1V, V_{GS} = 10 \text{ V})$ Each section side of device measured	Rds(on)	108		mΩ
Common Source Input Capacitance		430		
$(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$ Each section side of device measured	C _{ISS}	430		pF
Common Source Output Capacitance		100.7		_
(V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device measured	C _{oss}	100.7		pF
Common Source Feedback Capacitance	_	4.50		_
$(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$ Each section side of device measured	C _{RSS}	1.59		pF

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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1, 2—DRAIN, 3, 4—GATE, 5—SOURCE)



UNIT	A	b	С	D	D ₁	е	E	E ₁	F	Н	H ₁	L	р	Q	q	U ₁	U ₂	W ₁	W_2	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.05
111111	4.2	11.56	0.10	30.94	30.96	13.72	9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01	35.56	41.02	10.03	0.25	0.51	0.25
luabaa	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	4 400	1.625	0.405	0.04	0.00	0.04
inches	0.165	0.455	0.004	1.218	1.219	0.540	0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079	1.400	1.615	0.395	0.01	0.02	0.01

OUTLINE		REFERENCE		EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	1000E BATE
PKG-D4E					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status		
2018/04/20	Rev 1.0	Preliminary Datasheet		
2018/9/27	Rev 1.1	Rev 1.1 Update on power rating, Upper frequency limits, and Rth		
2019/12/25	Rev 1.2	Update on upper frequency limits, add FM test data according to RC		
		design		

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