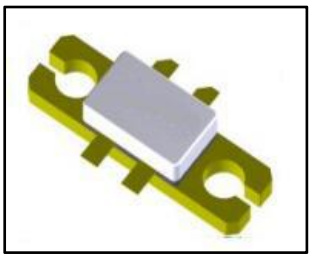
YC2002VP LDMOS TRANSISTOR

Document Number: YC2002VP
Preliminary Datasheet V1.0

20W, 50V RF Power LDMOS FETs

Description



The YC2002VP is a 20W capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 2GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF and UHF TV applications.

It can be configured as either push pull or single ended device.

- Typical performance(on 470-860MHz test board with device soldered): V_{DD} = 50 Volts,Vgs=3.43V, I_{DQ} = 50 mA, CW.

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	EFF(%)
470	24.2	43	20.0	0.93	18.8	42.9%
550	26.2	43	20.0	1.14	16.8	35.0%
650	26.2	43	20.0	1.16	16.8	34.4%
750	26.3	43	20.0	1.10	16.7	36.3%
860	25.5	43	20.0	1.06	17.5	37.6%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 470-860MHz (UHF TV)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	1.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃, half section, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0Ma	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600μA)	V_{GS}(th)	——	2.8	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 50 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.4	——	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)		1		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		11.4		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		4.9		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		0.05		pF

Load Mismatch (In YingtronTest Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 50 mA, f = 500MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 350W Pulsed CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram (Layout file upon request)

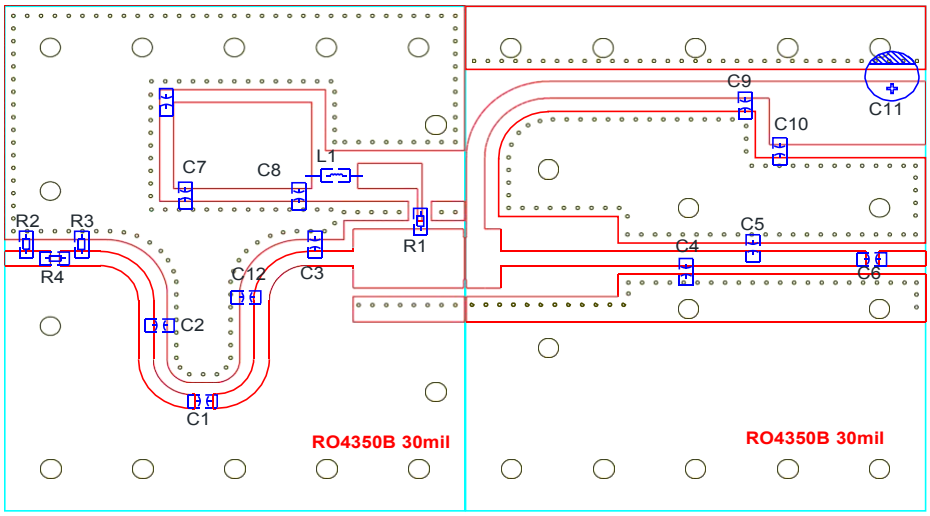


Figure 1. Test Circuit Component Layout (470-860MHz)

Table 1. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1, C6, C8, C9	470 pF	ATC800B
C2, C4, C5, C12	2.0 pF	ATC800B
C3	6.8 pF	ATC800B
R2, R3	Chip Resistor, 910Ω, 0805	
R4	Chip Resistor, 5.1Ω	
L1	25 nH	DIY
C7, C10	Electrolytic Capacitor ,10uF,50V	
R1	Chip Resistor,10Ω,0805	
PCB	0.762mm [0.030"] thick, εr=3.48, Rogers RO4350B, 1 oz. copper	

TYPICAL CHARACTERISTICS

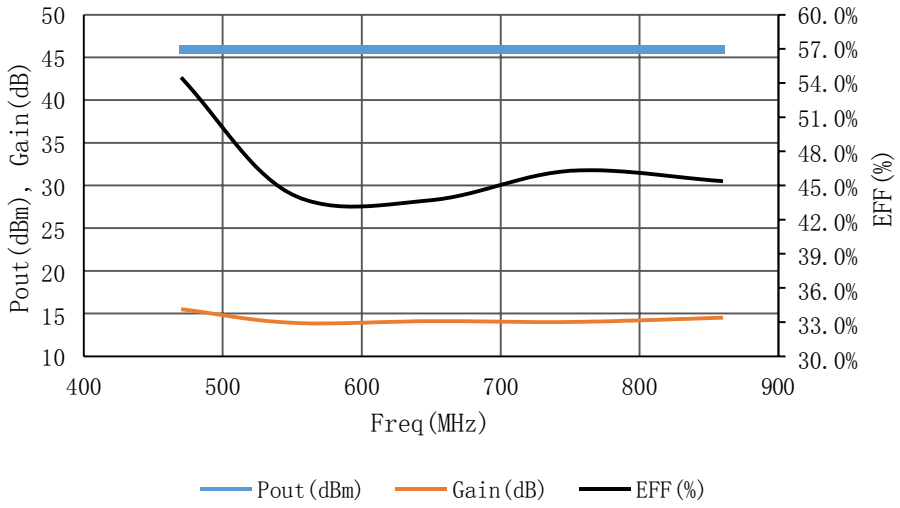


Figure 2: Pout, Power Gain and Drain Efficiency over the band

Test Condition:VDS=50V IDQ=50mA VGS=3.43VSignal mode: CW, Pout = Psat

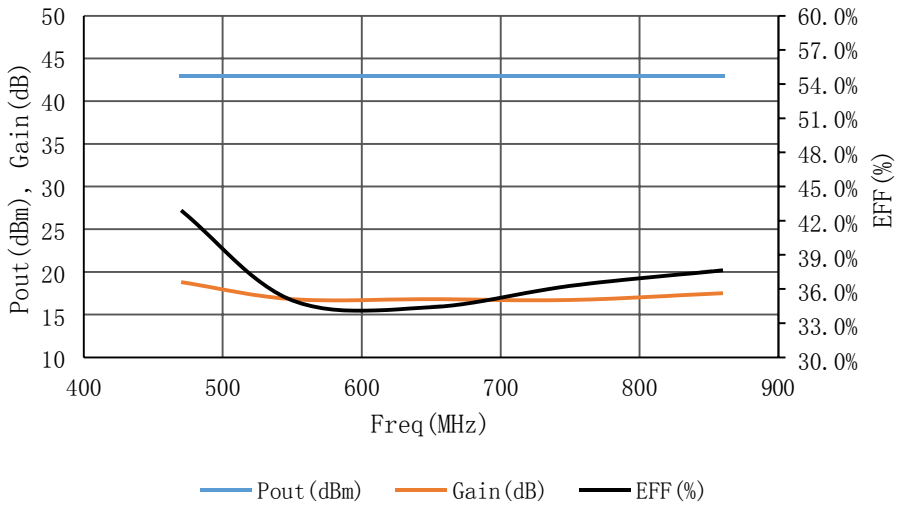
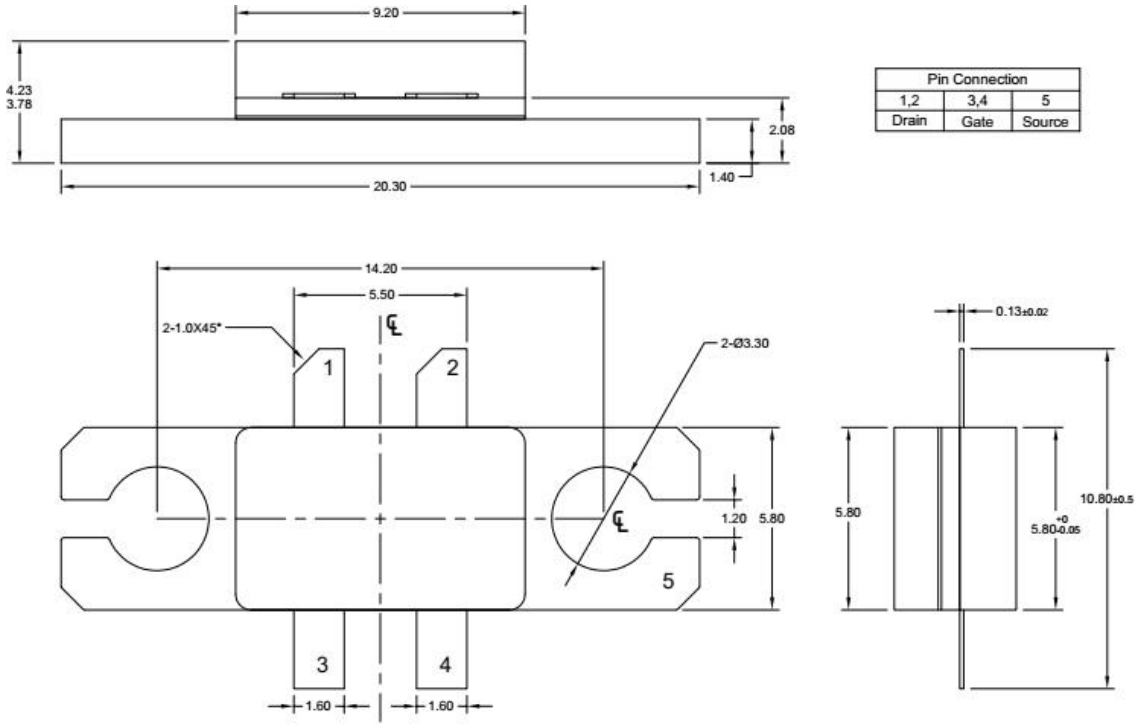


Figure 3:Pout, Power Gain and Drain Efficiency over the band

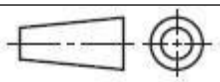
Test Condition:VDS=50V IDQ=50mA VGS=3.43VSignal mode: CW, Pout = 20W

Package Outline



Pin Connection		
1,2	3,4	5
Drain	Gate	Source

Unit：mm
Tolerances(unless specified)： x.x ±0.25
x.xx ±0.13

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-G4E					2018/01/19

Revision History

Table 6. Document revision history

Date	Revision	Datasheet Status
2019/11/30	Rev 1.0	Preliminary Datasheet Creation

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